REMARKS

In response to the Office Action mailed on April 12, 2007, Applicants respectfully request reconsideration based on the following remarks. Claims 1-29 are presently pending in the instant application. Applicants respectfully submit that the claims as presented are in condition for allowance.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Keltcher U.S. Patent 6,134,494 hereinafter referred to as "Keltcher", further in view of Nilsson, et al. U.S. Patent No. 6,973,547, hereinafter referred to as "Nilsson". Applicants respectfully traverse the rejection because Keltcher in view of Nilsson fails to teach or suggest all of the elements in Claim 1 - 29.

Claim 1, recites "A system for memory management, the system comprising: a tag controlled buffer in communication with a memory device, said memory device including a plurality of pages divided into a plurality of individually addressable lines, wherein said tag controlled buffer includes: a prefetch buffer including at least one of the individually addressable lines from the memory device; and a tag cache in communication with the prefetch buffer, the tag cache including at least one tag, wherein each said tag is associated with one of the pages in the memory device, each said tag includes a reference history field and a pointer to at least one line in the prefetch buffer that is from the associated page, access to the lines in the prefetch buffer is controlled by the tag cache, and the reference history field includes information about how the lines from the associated page have been accessed in the past and is utilized to determine which lines in the associated page should be added to the prefetch buffer when the tag is added to the tag cache", emphasis added.

Keltcher teaches a single size configurable data buffer that includes both data cache memory registers and a variable number of prefetch memory registers. The amount of space allocated to each register type can be modified by a computer controller (Keltcher; Abstract). In other words, a single size configurable data buffer SRAM device (12) can be internally partitioned to hold both data cache (32) and prefetch cache (34). (Keltcher; FIG. 1 and 2.)

Keltcher also teaches a TAG cache memory (18) to keep track of which lines from the main memory (24) are stored in the data cache and prefetch registers of the data buffer cache SRAM device (12). (Keltcher; FIG. 1.) The TAG cache memory (18) of Keltcher includes one line of address information (a 20 bit TAG) per line of data in the data buffer cache SRAM device (12), which is 128 lines in the example of FIG. 1. When the controller (22) generates an address desired from the main memory (24), an address comparison is performed with the contents of the TAG cache memory (18) and the address recovery SRAM (16) to determine whether the desired contents are presently in the data buffer cache SRAM device (12). (Keltcher; col. 3, lines 28-40.) The TAG cache memory (18) TAGs hold the upper 20 bits of the memory address, which is equal to the upper 20 bits of the main memory (24) address that correspond to the data stored in the data buffer cache SRAM device (12). (Keltcher; col. 3, line 49 – col. 4, line 29.) Thus, in Keltcher, when the controller (22) generates a desired 32-bit address, it can potentially locate the data within the data buffer cache SRAM device (12) by routing the upper 20 address bits to the TAG cache memory (18), where the 20 bits may correspond to the contents of a TAG, and route the lower 12 address bits to the data buffer cache SRAM device (12) as row and column addresses within the data buffer cache SRAM device (12) to select the data located therein via the address recovery SRAM (16). In other words, each TAG in Keltcher **does not include** a "pointer to at least one line in the prefetch buffer", as recited in Claim 1; rather, each TAG in Keltcher is the upper 20 address bits of either a line of the data cache (32) or a line of the prefetch cache (34) for mapping the contents of the data buffer cache SRAM device (12) back to the main memory (24). Thus, the "pointer" address in each TAG in Keltcher actually points the main memory (24) address that corresponds to the data stored in the data buffer cache SRAM device (12).

Moreover, Keltcher does not teach or suggest a "memory device including a plurality of **pages**", as recited in Claim 1. Therefore, Keltcher does not teach or suggest that "each said tag is **associated with one of the pages** in the memory device", as recited in Claim 1. Additionally, Keltcher does not teach or suggest that "access to the lines in the prefetch buffer is controlled by the tag cache", as recited in Claim 1. Rather, Keltcher teaches that the **controller (22) controls access** to the prefetch cache (34) of the data buffer cache SRAM device (12). (Keltcher; col. 4, lines 42-43.) Thus, Keltcher fails to teach or suggest all of the elements of Claim 1.

As stated above, Keltcher fails to disclose all of the elements of Claim 1. The addition of Nilsson fails to cure these deficiencies. Nilsson teaches a coherence message prediction mechanism for multiprocessing computer systems including a history cache for storing a plurality of cache entries, each storing coherence history information for a corresponding block of data. The entries in the history cache are used to index into a pattern memory containing coherence predictions. (Nilsson; col. 2, lines 31-38). Nilsson does not teach or suggest prefetching or a prefetch buffer, and thus fails to cure the deficiencies of Keltcher. Further, the history cache in Nilsson holds access messages identifying which processor in a multi-processor system performed an access type to a data block, but Nilsson does not teach or suggest "the reference history field includes information about how the lines from the associated page have been accessed in the past", as recited in Claim 1. Moreover, Nilsson does not teach or suggest that the reference history field "is utilized to determine which lines in the associated page should be added to the prefetch buffer when the tag is added to the tag cache", as recited in Claim 1. Therefore, Nilsson does not cure the deficiencies of Keltcher with respect to Claim 1. Accordingly, neither Keltcher nor Nilsson, alone or in combination, teaches or suggests all of the elements of Claim 1.

In reference to Claim 14, Keltcher does not teach or suggest that "each line is associated with **a page** in a memory device", and "each tag corresponds to **one of the pages** in the memory device, each tag indicates the location in the random access memory of the at least one line associated with the page", as recited in Claim 14. As previously discussed, Keltcher does not teach or suggest paged memory. The TAGs in Keltcher represent the upper 20 address bits of the main memory (24) address for the contents of each line in the data buffer cache SRAM device (12), and as such, the contents of each TAG can be the same for any number of TAGs, without "each tag correspond[ing] to one of the pages" as recited in Claim 14. Thus, Keltcher fails to teach or suggest all of the elements of Claim 14. Similar to Claim 1, Nilsson fails to cure these deficiencies. Again, Nilsson does not teach or suggest that a "reference history field that includes information about how lines in the associated page in the memory device have been accessed in the past and is utilized to determine which lines from the associated page should be added to the random access memory when the tag is added to the first cache device", as recited

in Claim 14. Therefore, Nilsson does not cure the deficiencies of Keltcher with respect to Claim 14. Accordingly, neither Keltcher nor Nilsson, alone or in combination, teaches or suggests all of the elements of Claim 14.

In reference to Claims 2-20, 12-13, and 15-23, Claims 2-13 depend from Claim 1, and thus are believed to be allowable at least due to their dependency on Claim 1. Claims 15-23 depend from Claim 14, and thus are believed to be allowable at least due to their dependency on Claim 14.

Claims 11 and 24-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Keltcher, further in view of Nilsson, as applied to claim 1 above, and further in view of Dean U.S. Patent No. 5,544,342, hereinafter referred to as "Dean".

As stated above, Keltcher and Nilsson, alone or in combination, fail to disclose all of the elements of Claim 1, from which Claim 11 depends. In addition, Dean fails to cure these deficiencies. Dean also fails to teach or suggest at least the elements "the fault notification including a fault page identifier and a fault line identifier", as recited in Claim 11. Dean merely states that a fetch to the next level of a memory hierarchy is initiated in response to a cache miss. (Dean; col. 31, lines 57-62.) There is no teaching or suggestion of both a "a fault page identifier and a fault line identifier" in Dean. Accordingly, Keltcher, Nilsson, and Dean, alone or in combination, fail teach or suggest all of the elements of Claim 11.

In reference to Claims 24, 25, and 29, as described above, with respect to Claims 1, 11, and 14, Keltcher, Nilsson, and Dean (the References) fail to teach or suggest multiple elements. Specifically, the References fail to teach or suggest "a reference history field that includes information about how lines in the corresponding page have been accessed in the past" and "the fault notification including a fault page identifier and a fault line identifier", as recited in Claims 24, 25, and 29. Moreover, the References fail to teach or suggest that each tag includes "at least one pointer to lines in a prefetch buffer", as recited in Claims 25 and 29. Therefore, Dean does not cure the deficiencies of Keltcher and Nilsson with respect to Claims 24, 25, and 29. Accordingly, Keltcher, Nilsson, and Dean, alone or in combination, fail teach or suggest all of the elements of Claims 24, 25, and 29.

Claims 26-28 depend from Claim 25, and thus are believed to be allowable at least due to their dependency on Claim 25.

Conclusion

Allowance of the claims is respectfully requested in view of the above remarks. Moreover, no amendments have been presented that alter the scope of the claimed invention, and therefore cannot necessitate a new grounds rejection.

It is believed that the foregoing remarks are fully responsive to the Office Action and that the claims herein should be allowable to Applicants. In the event the Examiner has any queries regarding the instantly submitted response, the undersigned respectfully request the courtesy of a telephone conference to discuss any matters in need of attention.

If there are any charges with respect to this response or otherwise, please charge them to Deposit Account 50-0510 maintained by Applicants' attorneys.

Respectfully submitted,
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